ABSTRACT

A circuit is disclosed for controlling power supplied to a pipelined circuit. The circuit includes a front-end transition detection circuit, a back-end transition detection circuit and a stage power control circuit. The stage power control circuit includes a timer that may be reset in response to the back-end transition detection circuit detecting a transition in the output of the pipelined circuit. If the timer expires, the stage power control circuit performs a shut-down procedure that includes sequentially suppressing power to a plurality of stage circuits in the pipelined circuit. The sequential suppression of power includes suppressing power provided to a first stage circuit at the end of a first clock cycle, and the first stage circuit is connected to the input of the pipelined circuit. Then, power supplied to a second stage circuit directly connected to the first stage circuit may be suppressed after the next clock cycle. The sequential shut-down procedure may continue until power is suppressed for all the stage circuits in the pipelined circuit, and thus the power consumed by the pipelined circuit is minimized. The stage control circuit may also perform a turn-on procedure for providing power to the stage circuits that have had power suppressed during the shut-down procedure. If the front-end detection circuit detects the transition of a signal transmitted to the pipelined circuit, then the turn-on procedure is performed. The turn-on procedure may be performed even if all the stage circuits have not had their power supply suppressed. The turn-on procedure includes sequentially providing power to the stage circuits, starting from the first stage circuit.